with the driving circuit wherein said integrated circuit chip is at least one of a memory, an input port, a correction memory and a CPU,

wherein said at least one thin film transistor and said at least another one thin film transistor are formed from a common semiconductor film formed over the first surface of the insulating substrate, and

wherein said at least one thin film transistor of the active matrix circuit has at least one lightly doped drain between a channel region and a drain region thereof.

REMARKS

The Official Action mailed January 17, 2002 has been received and its contents carefully noted. Filed concurrently herewith is a *Request for a One Month Extension of Time*, which extends the shortened period for response to May 17, 2002. Accordingly, Applicant respectfully submits that this response is being timely filed.

Claims 1-7, 9, 10, 17-24, 26, 27 and 30-55 were pending in the present application. By this amendment, claims 32, 36, 38 and 51 have been amended and claims 4, 5, 34 and 35 have been canceled. Accordingly, claims 1-3, 6, 7, 9, 10, 17-24, 26, 27, 30-33 and 36-55 remain pending, of which claims 1, 7, 17, 21, 32, 36, 38 and 51 are independent.

The Examiner has indicated that the Information Disclosure Statement (IDS) filed October 24, 2000 fails to comply 37 CFR 1.98(a)(2) requiring legible copies of the references and all other information which caused it to be listed. The Applicants also note that two publications (Joannopoulos et al. and Lewis et al.) from the IDS dated December 20, 2000 were not considered by the Examiner for presumably the same reason. In response, the Applicants have provided copies of many of the references herewith and are in the process of obtaining legible copies of the remaining references for consideration by the Examiner and will submit these references shortly. Applicant respectfully requests the Examiner to carefully review these references, initial the PTO

1449 previously provided for each reference, and return an initialed copy with the subsequent Official Action.

Paragraph 3 of the Official Action rejects claims 7, 9, 10, 17-19, 27, 30, 51, 52 and 54 as anticipated by U.S. Patent 5,581,092 to Takemura. The Applicants respectfully traverse the Examiner's rejection. Takemura does not teach or suggest all the elements of the independent claims, either explicitly or inherently.

Independent claims 7, 17 and 51 recite that at least one semiconductor integrated circuit chip of at least one of a memory, an input port, a correction memory, and a CPU is provided over a substrate of the electric device or the display device as shown in Fig. 3, and the substrate comprises an active matrix circuit and a driving circuit both including thin film transistors.

In the previous response, Applicants asserted that Takemura fails to teach a semiconductor integrated circuit chip since Takemura discloses a thin film semiconductor IC. In the pending Office Action, the Examiner contends that the same is true of Takemura's IC and cites column 14, lines 56-57. However, as taught in column 14, lines 56-63 of Takemura, an input port, a correction memory, a memory, and a CPU are constituted by TFTs and are formed on the same substrate as an X-decoder/driver, a Y-decoder/driver, and an X-Y divider. On the other hand, the present invention as recited in claims 7, 17 and 51 includes at least one semiconductor integrated circuit chip as shown by reference numerals 36-38 of FIG. 3 and these chips are not constituted by TFTs.

For the reasons stated above, it is respectfully submitted that Takemura fails to disclose each and every element of the presently claimed invention and reconsideration and withdrawal of the rejection of independent claims 7, 17 and 51 is respectfully requested. Likewise, it is believed that dependent claims 9, 10, 18, 19, 27, 30, 52 and 54 are likewise allowable in that they depend from what is believed to be allowable base claims 7, 17 and 51.

Paragraph 5 of the Official Action rejects claims 20, 45, 46 and 55 as obvious based on Takemura, as stated in the previous Office Action. The Applicants respectfully traverse the Examiner's rejection because the Examiner has not made a *prima facie* case of obviousness.

Please incorporate the arguments above with respect to the deficiencies in Takemura. The knowledge available to one with ordinary skill in the art does not cure the deficiencies in Takemura. The prior art, either alone or in combination, does not teach or suggest that at least one semiconductor integrated circuit chip of at least one of a memory, an input port, a correction memory, and a CPU is provided over a substrate of the electric device or the display device, and the substrate comprises an active matrix circuit and a driving circuit both including thin film transistors. Furthermore, there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Takemura to achieve the claimed invention.

For the reasons stated above, the Examiner has not set forth a *prima facie* case of obviousness. Accordingly, reconsideration and withdrawal of the rejection of dependent claims 20, 45, 46 and 55 under 35 U.S.C. § 103(a) is in order and respectfully requested.

Paragraph 6 of the Official Action rejects claims 1-7, 9, 10, 17-24, 26, 27, 30-35, 38-41, 43-48 and 50-55 as obvious based on the combination of Takemura and U.S. Patent 5,148,301 to Sawatsubashi. As noted above, claims 4, 5, 34 and 35 have been canceled, and thus the rejection of these claims is moot. The Applicants respectfully assert that the Official Action has failed to establish a *prima facie* case of obviousness.

Please incorporate the arguments above with respect to the deficiencies in Takemura. Sawatsubashi does not cure the deficiencies in Takemura. The prior art, either alone or in combination, does not teach or suggest all the elements of the independent claims. Independent claims 1, 7, 17, 21, 32, 38 and 51 recite that at least one semiconductor integrated circuit chip of at least one of a memory, an input port, a

correction memory, and a CPU is provided over a substrate of the electric device or the display device as shown in Fig. 3, and the substrate comprises an active matrix circuit and a driving circuit both including thin film transistors.

Sawatsubashi also fails to teach the semiconductor integrated circuit chip, so that the claimed invention of claims 1, 7, 17, 21, 32, 38 and 51 cannot be obtained even if motivation could be found to combine Takemura and Sawatsubashi.

Independent claim 36 recites that each thin film transistor in an active matrix circuit is a bottom gate type transistor, and each thin film transistor in a driving circuit is a top gate type transistor, which is supported in Fig. 11D. The Official Action asserts U.S. Patent No. 5,121,236 to Ukai or U.S. Patent No. 5,223,961 to Ukai for providing evidence of the limitation of "a bottom gate" and "a top gate." However, neither Ukai '236 nor Ukai '961 discloses that the active matrix circuit has a bottom gate type thin film transistor and the driving circuit has a top gate type thin film transistor as mentioned above. Hence, the Applicants respectfully submit that Ukai '236 and Ukai '961 do nothing to overcome the above deficiencies and do not render claim 36 obvious.

For the reasons stated above, the Examiner has not set forth a *prima facie* case of obviousness. Accordingly, reconsideration and withdrawal of the rejection of independent claims 1, 7, 17, 21, 32, 38 and 51 is respectfully requested. Likewise, it is believed that dependent claims 2, 3, 6, 9, 10, 18-20, 22-24, 26, 27, 30, 31, 33, 39-41, 43-48, 50 and 52-55 are likewise allowable in that they depend from what is believed to be allowable base claims 1, 7, 17, 21, 32, 38 and 51.

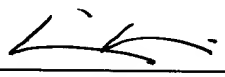
Paragraph 7 of the Official Action rejects claims 1-7, 9, 10, 17-24, 26, 27, 30-35, 38-41, 43-48 and 50-55 under the judicially created doctrine of obviousness-type double patenting based on claims 3, 13 and 17 of U.S. Patent No. 5,889,291. As noted above, claims 4, 5, 34 and 35 have been canceled. The remaining rejected claims recite that the semiconductor integrated circuit chip is at least one of a memory, an input port, a correction memory, and a CPU. On the other hand, the '291 patent merely recites a semiconductor chip. Therefore, the Applicants respectfully submit that the subject

memory chip 26, correction 28

application is patentably distinct from the '291 patent, and the double patenting rejection should be withdrawn.

For all of the above reasons, the present application is believed to be in condition for allowance and favorable reconsideration is respectfully requested. If the Examiner feels further discussions would expedite prosecution of this application, he is invited to contact the undersigned.

Respectfully submitted,



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MARKED-UP VERSION OF THE AMENDED CLAIMS

32. (Amended) A display device comprising:

a first substrate having an insulating surface;

an active matrix circuit including a first plurality of thin film transistors formed on the insulating surface of the first substrate;

a driving circuit including a second plurality of thin film transistors formed over the insulating surface of the first substrate for driving said active matrix circuit;

a second substrate facing said first substrate with a liquid crystal material interposed therebetween, said first substrate having an extended portion which extends beyond at least one side edge of the second substrate wherein said second substrate covers said active matrix circuit and said driving circuit; and

at least one semiconductor integrated circuit chip disposed over the extended portion of the first substrate and operationally connected to said driving circuit wherein said integrated circuit chip is at least one of a memory, an input port, a correction memory and a CPU,

wherein said first and second plurality of thin film transistors are formed from a common semiconductor film formed over said first substrate, and each of said first plurality of thin film transistors has at least one lightly doped drain between a channel region and a drain region thereof.

36. (Amended) A display device comprising:

a first substrate having an insulating surface;

an active matrix circuit including a first plurality of thin film transistors formed on the insulating surface of the first substrate;

a driving circuit including a second plurality of thin film transistors formed over the insulating surface of the first substrate for driving said active matrix circuit;

a second substrate facing said first substrate with a gap therebetween, said first substrate having an extended portion which extends beyond at least one side

edge of the second substrate wherein said second substrate covers said active matrix circuit and said driving circuit; and

at least one semiconductor integrated circuit chip disposed over the extended portion of the first substrate and operationally connected to said driving circuit,

wherein each of said first plurality of thin film transistors is a bottom gate type transistor in which a gate electrode is located below a channel region of the transistor, and each of said second plurality of thin film transistors is a top gate type transistor in which a gate electrode is located over a channel region of the transistor.

38. (Amended) A display device comprising:

a first substrate having an insulating surface;

an active matrix circuit including a first plurality of thin film transistors formed on the insulating surface of the first substrate;

a driving circuit including a second plurality of thin film transistors formed over the insulating surface of the first substrate for driving said active matrix circuit; and

a second substrate facing said first substrate with a gap therebetween, said first substrate having an extended portion which extends beyond at least one side edge of the second substrate;

at least one semiconductor integrated circuit chip disposed over the extended portion of the first substrate and operationally connected to said driving circuit,

wherein said semiconductor integrated circuit chip is selected from the group consisting of a correction memory, a memory, a CPU, and an input port.

51. (Amended) An electric device comprising:

an insulating substrate;

an active matrix circuit including at least one thin film transistor formed over a first surface of said insulating substrate;

a driving circuit including at least another one thin film transistor for driving the active matrix circuit formed over said first surface of the insulating substrate; and

at least one semiconductor integrated circuit chip disposed over said first surface of the extended portion of the insulating substrate and operationally connected with the driving circuit wherein said integrated circuit chip is at least one of a memory, an input port, a correction memory and a CPU,

wherein said at least one thin film transistor and said at least another one thin film transistor are formed from a common semiconductor film formed over the first surface of the insulating substrate, and

wherein said at least one thin film transistor of the active matrix circuit has at least one lightly doped drain between a channel region and a drain region thereof.